REMARKS

Claims 22, 27, 34, 38, 41, 45, 49, 52, 61, 65, 72, and 75 are amended; as a result, claims 22-55, 57-69, 72 and 75 are now pending in this application. Claims 56, 70, 71, 73, 74, 76, and 77 were previously cancelled in a response to the April 9, 2003 Office Action.

Examiner Interview Summary

The undersigned thanks the examiner for the courtesy shown in a telephone interview of February 9, 2004. The undersigned informed the examiner of the two fax requests for identification of the Tobita document used in the Office Action to reject the claims and to restart the time period of a response. Examiner Wojciechowicz provided the U.S. Patent Number for the Tobita document (5,646,516) and agreed to restart the time period for a response.

Applicant requests that the present response be entered without charging the application a time extension fee as the failure of the USPTO to include the form PTO-892 that provided the only location of the patent number for the Tobita document was the reason for the delay in the response. However, applicant will allow the USPTO to charge deposit account no. 19-0743 if the fee must be paid to have this paper entered into the USPTO record. If the fee is charged, applicant will request a refund due the USPTO error.

Reservation of the Right to Swear Behind References

Applicant maintains its right to swear behind any references which are cited in a rejection under 35 U.S.C. §§102(a), 102(e), 103/102(a), and 103/102(e). Statements distinguishing the claimed subject matter over the cited documents are not to be interpreted as admissions that the documents are prior art.

§112 Rejection of the Claims

Claims 22-77 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention, for the reasons given in the previous action, hereby incorporated by reference.

Claims 22, 27, 34, 38, 41, 45, 49, 52, 61, 65, 72, and 75 were amended to better recite the subject matter. Applicant believes the present claims are in a form allowable under 35 U.S.C. § 112 second paragraph.

§102 Rejection of the Claims

Claims 22-77 were rejected under 35 U.S.C. § 102(a) as being anticipated by Tobita (U.S. Pat. No. 5,646,516). Applicant respectfully traverses the rejection because Tobita does not disclose all of the elements recited in the contested claims.

Regarding claims 22-26:

Applicant is unable to find in the cited portions of Tobita, among other things, any disclosure of, providing an output voltage at an output of the transistor, the output voltage equal to the applied voltage reduced by a threshold voltage of the transistor, wherein the output of the transistor is coupled to a well that bounds the transistor, as presently recited or incorporated in the claims.

Regarding claims 27-29:

Applicant is unable to find in the cited portions of Tobita, among other things, any disclosure of, providing an output voltage at a second source/drain of the transistor and a well bounding the transistor, as presently recited or incorporated in the claims.

Regarding claims 30-33:

Applicant is unable to find in the cited portions of Tobita, among other things, any disclosure of, coupling a well, that isolates the transistor from a substrate, to the circuit, as recited or incorporated in the claims.

Regarding claims 34-37:

Applicant is unable to find in the cited portions of Tobita, among other things, any disclosure of, providing an output voltage at a second source/drain of the transistor, the output voltage equal to the applied voltage reduced by the threshold voltage of the transistor, wherein a semiconductor region containing the first and second source/drains is coupled to the second source/drain of the transistor, as presently recited or incorporated in the claims.

Regarding claims 38-40:

Applicant is unable to find in the cited portions of Tobita, among other things, any disclosure of, isolating the transistor from a substrate region of the integrated circuit by a well formed in the substrate region; and coupling the well to the internal circuit, as presently recited or incorporated in the claims.

Regarding claims 41-44:

Applicant is unable to find in the cited portions of Tobita, among other things, any disclosure of, providing an output voltage at an output of the second transistor, the output voltage equal to the applied voltage reduced by a threshold voltage of the first transistor and a threshold voltage of a second transistor, and wherein a well, bounding the first transistor and the second transistor, is coupled to the output, as presently recited or incorporated in the claims.

Regarding claims 45-48:

Applicant is unable to find in the cited portions of Tobita, among other things, any disclosure of, providing an output voltage at an output of the second transistor, the output voltage equal to the applied voltage reduced by a threshold voltage of both the first transistor and the second transistor, and wherein a first well, bounding the first transistor, is coupled to the second transistor and a second well, bounding the second transistor, is coupled to the output, as presently recited or incorporated in the claims.

Regarding claims 49-54:

Applicant is unable to find in the cited portions of Tobita, among other things, any disclosure of, providing an output voltage at a second source/drain of the second transistor, wherein the output voltage is reduced from the applied voltage by a threshold voltage of both the first transistor and the second transistor, as presently recited or incorporated in the claims.

Regarding claims 55, 57-60:

Applicant is unable to find in the cited portions of Tobita, among other things, any disclosure of, a semiconductor region of the transistor containing the first and second source/drains is coupled to the node, as recited or incorporated in the claims.

Regarding claims 61-64:

Applicant is unable to find in the cited portions of Tobita, among other things, any disclosure of, biasing a well of the transistor to a second source/drain, as presently recited or incorporated in the claims.

Regarding claims 65-68:

Applicant is unable to find in the cited portions of Tobita, among other things, any disclosure of, wherein the output of the transistor is coupled to a well that isolates the transistor from a substrate of the integrated circuit, as presently recited or incorporated in the claims.

Regarding claim 69:

Applicant is unable to find in the cited portions of Tobita, among other things, any disclosure of, applying the reduced voltage to the at least one internal circuit, wherein a well that isolates the transistor from a substrate of the integrated circuit is coupled to the at least one internal circuit, as recited in claim 69.

Regarding claim 72:

Applicant is unable to find in the cited portions of Tobita, among other things, any disclosure of, applying the reduced voltage to the at least one internal circuit, wherein a semiconductor region containing the first and second source/drains and common source/drain of the first and second transistors is coupled to the at least one internal circuit, as presently recited in claim 72.

Regarding claim 75:

Applicant is unable to find in the cited portions of Tobita, among other things, any disclosure of, a first semiconductor region containing the first and second source/drains of the first transistor is coupled to the first source/drain and the gate of the second transistor and wherein a second semiconductor region containing the first and second source/drains of the second transistor is coupled to the at least one internal circuit, as presently recited in claim 75.

Therefore, because Tobita does not disclose all of the elements recited in the contested claims, Applicant respectfully requests reconsideration and allowance of claims 22-55, 57-69, 72 and 75.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 3 March '04

By _____
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 3rd day of March, 2004.

Amy Moriarty
Name

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Signature